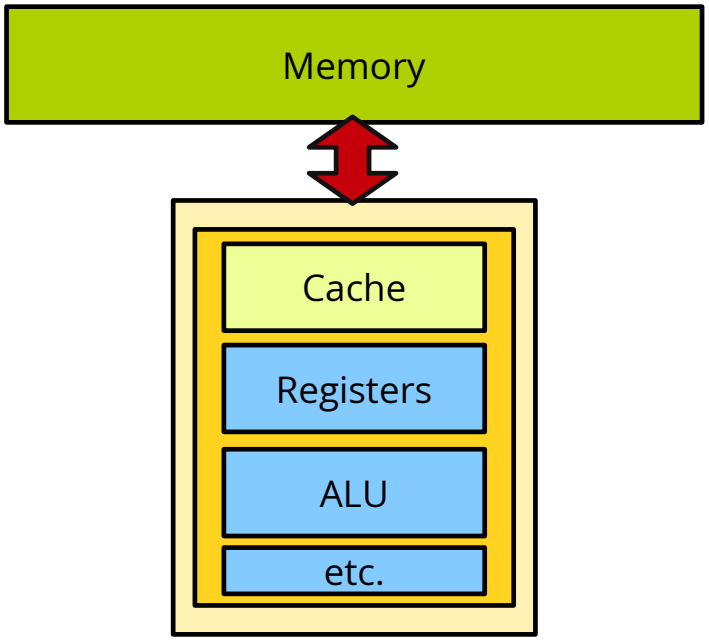
MANCHESTER 1824
The University of Manchester

COMP35112 Chip Multiprocessors

Introduction 1

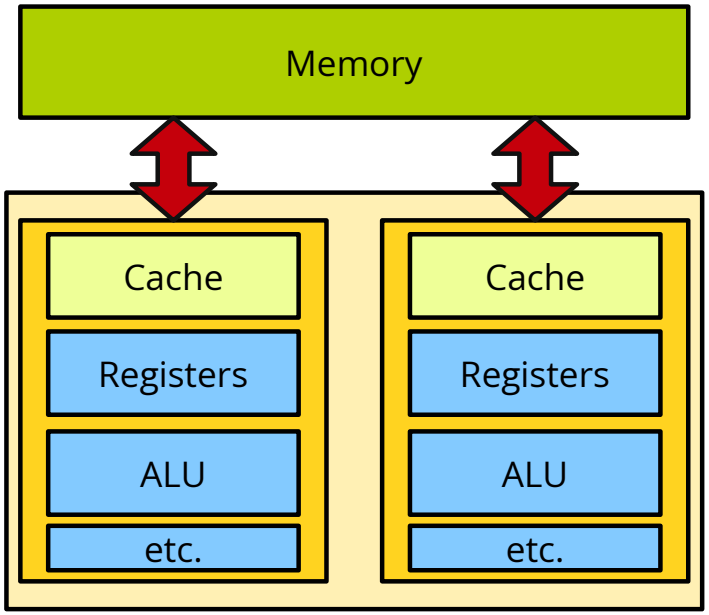
Pierre Olivier

Chip Multiprocessors?



Uniprocessor or single-core CPU

Chip Multiprocessors?



Multiprocessor or multicore CPU

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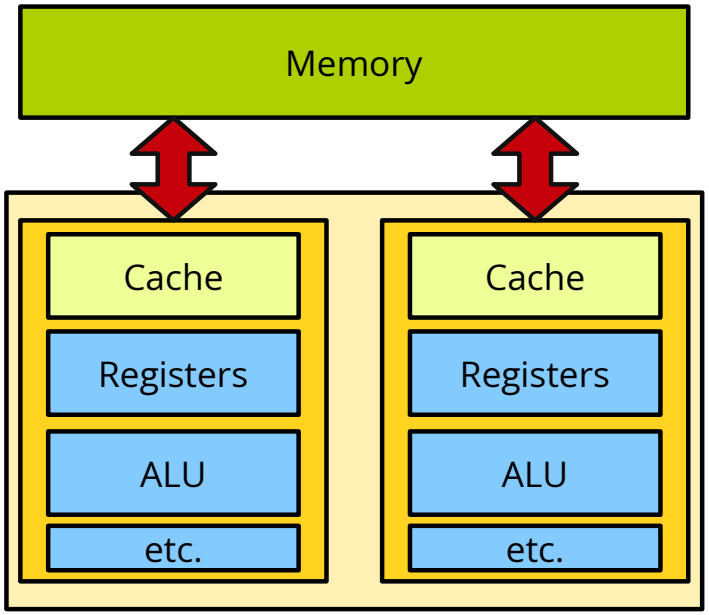
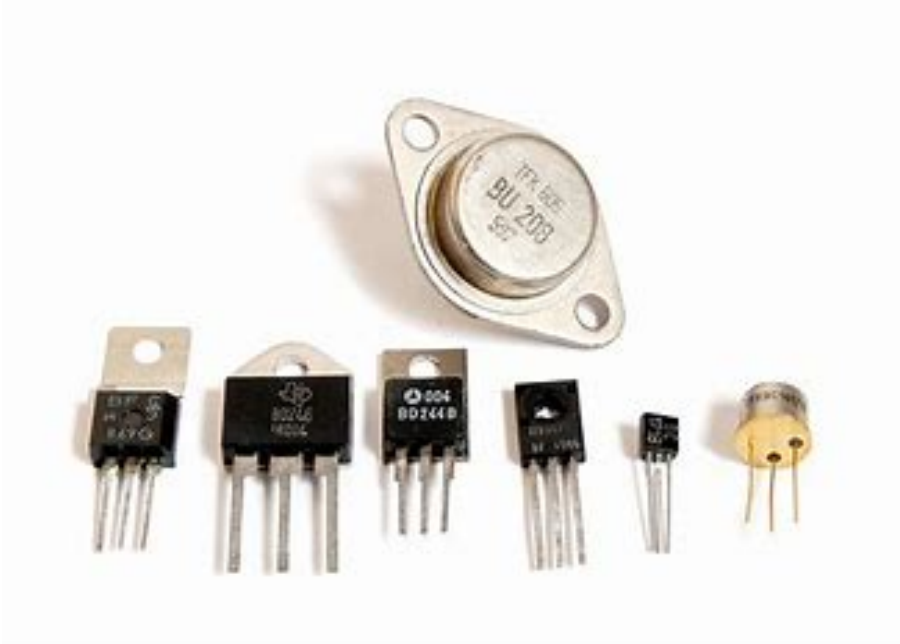


Multiprocessor or multicore CPU

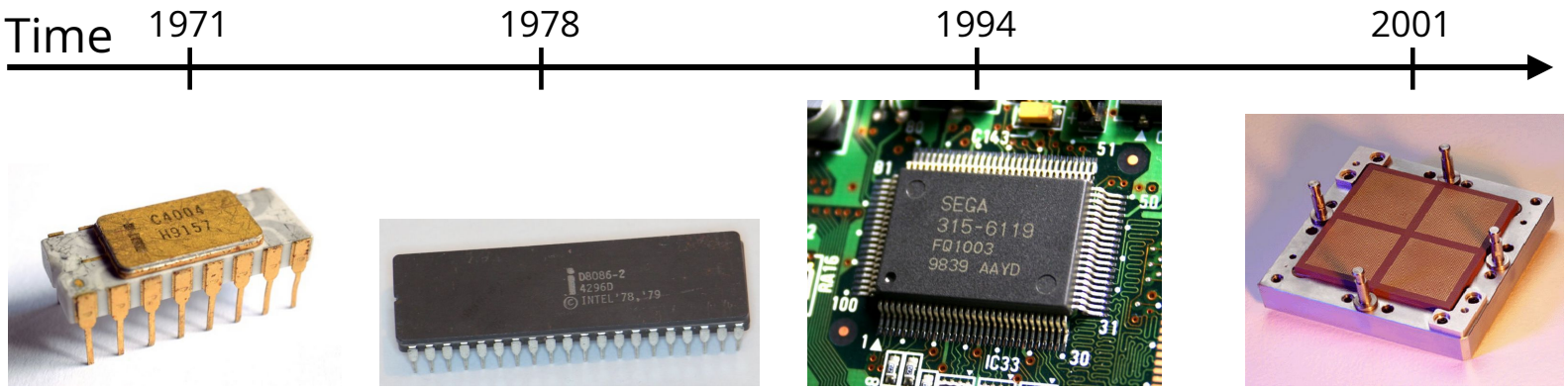
Why was this invented?

Chip Multiprocessors?



Chip Multiprocessors?

- Computing power of a CPU is function of the number of transistors it integrates



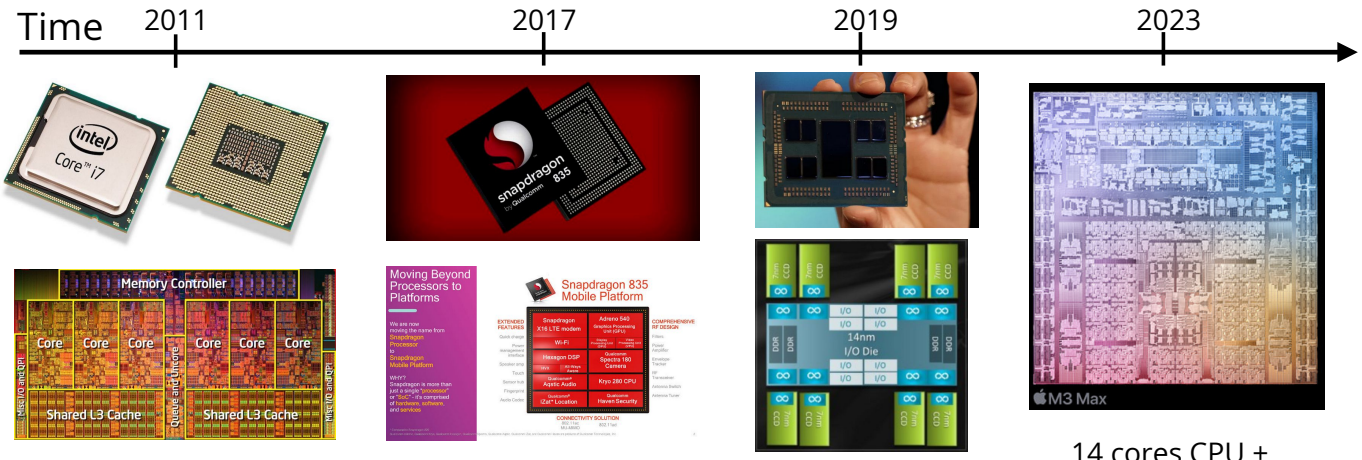
Intel 4004
1st commercial IC processor,
2,300 transistors

Intel 8086,
30K transistors

ARM7,
600K transistors

IBM Power4,
170M transistors,
2 cores

Chip Multiprocessors?



6 cores Intel i7, ~1.1 Billion transistors

Qualcomm Snapdragon 835 SoC (Quad core, GPU, DSP...), ~3 Billion transistors

64 cores AMD EPYC Rome, 40 Billion transistors

14 cores CPU + 18 cores GPU Apple M3 Max, 92 Billion transistors

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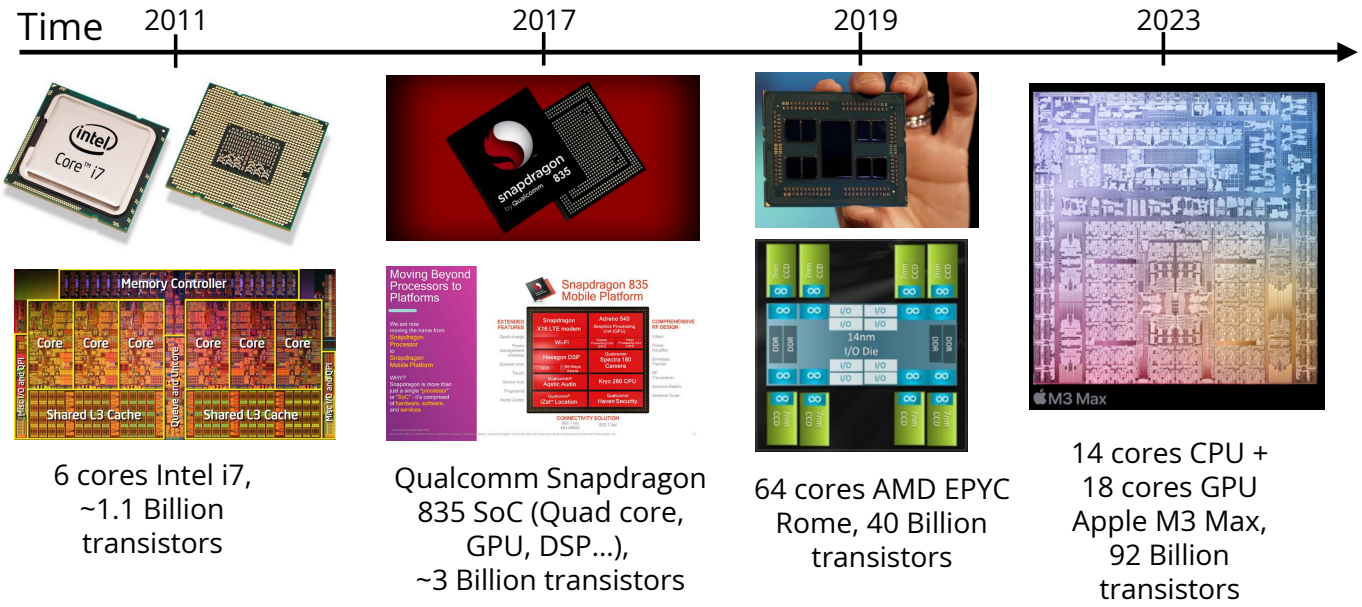

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Why this increase in number of compute units (cores) per chip?

Core Count Increase

- For decades we have seen a continual increase in single-core processors **speed**
- Transistors get (significantly) smaller, circuits get (a bit) bigger, **clock frequency increase**
  - Program is slow? Wait for the next generation CPU to get an automatic speed boost ➡️ free lunch for the programmer

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- Power consumption and heat dissipation → **clock speed stalled**
- **Architectural approaches to increase single processor speed have been exhausted**

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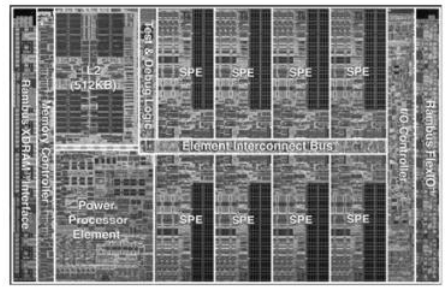
  - **Software issues**: how do we program this thing?



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  - Feature size (basically transistor size)
    - Intel 386 (1985): 1.5 um
    - Apple M1 Max (2021): 5 nm
    - Decrease factor: 300x
  - Die (chip) size
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- Increase in transistors/chip mostly due to **transistor size reduction**

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  - Smaller transistors have a faster switch delay
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- **But we hit limits**
  - Power density increases, heating becomes a problem

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  - **Broke down in the mid-2000s** 🥲
    - Mostly due to the high current leakage with small transistor sizes

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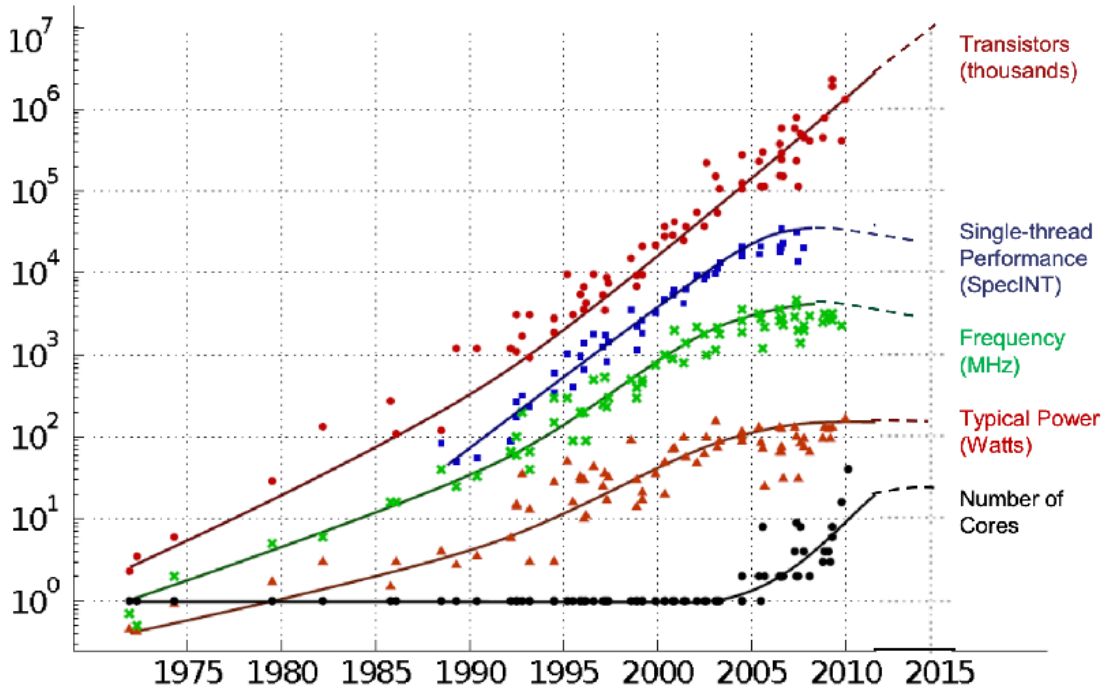
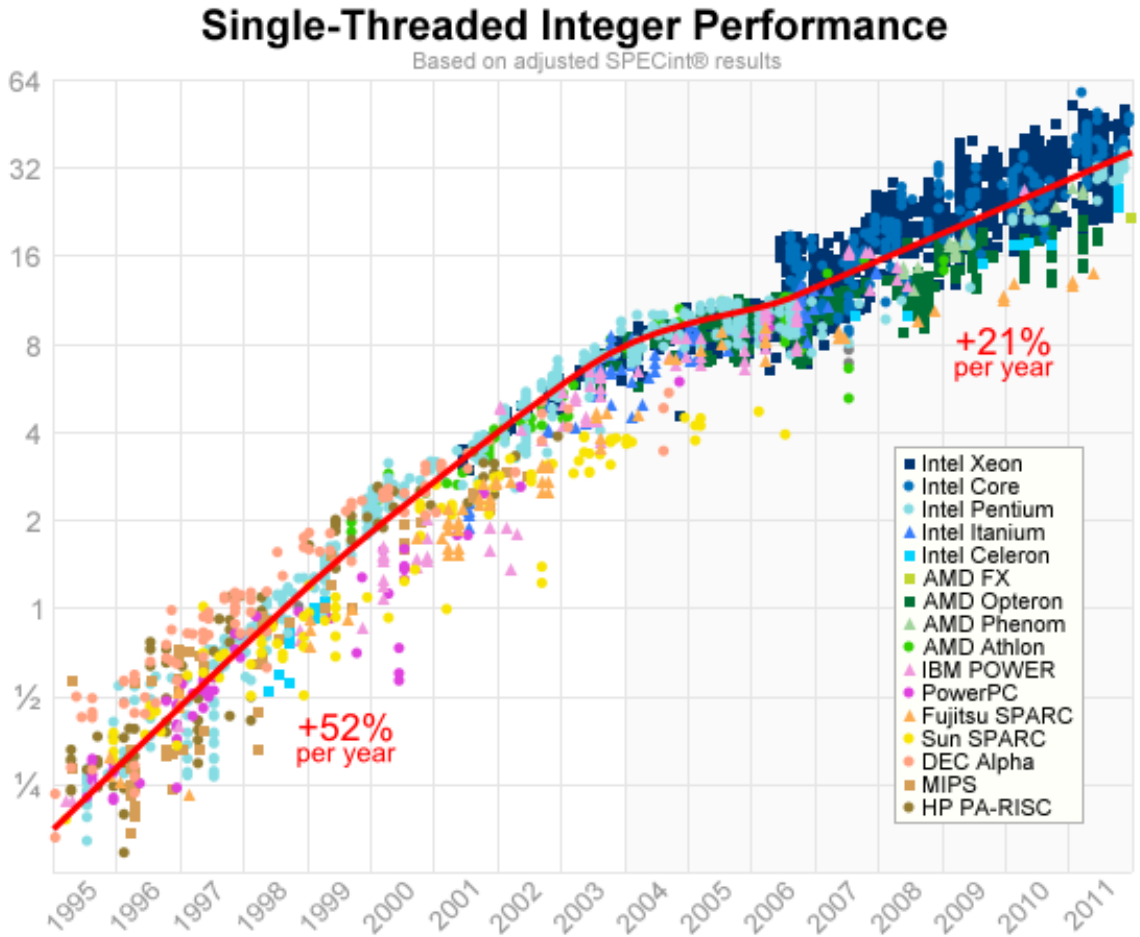


Original data collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond and C. Batten
Dotted line extrapolations by C. Moore

End of Dennard Scaling: Frequency can't keep increasing because power can't be removed from the chips, they'd melt!

Single Core Performance



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    - **More parallel pipelines** to exploit Instruction Level Parallelism?
      - ILP has diminished returns beyond ~4 pipelines
    - **Bigger caches**:
      - Payback for bigger caches also diminishes rapidly

The "Solution": Multiple Cores

- Put multiple CPUs (cores) on a single integrated circuit (chip)
  - **"Multicore chip" or "Chip Multiprocessor"**
- Use these CPUs in parallel to achieve higher performance
- Simpler to design vs. increasingly complex single core CPUs
- Need more computing power? Add more cores ...
  - ... not that simple in practice, 2 * 3GHz != 6GHz

Multicore "Roadmap"

- Year, cores per chip, feature size

- 2006, ~2 cores, 65nm
- 2008, ~4 cores, 45nm
- 2010, ~8 cores, 33nm
- 2012, ~16 cores, 23nm
- 2014, ~32 cores, 16nm
- 2016, ~64 cores, 12nm
- 2018, ~128 cores, 8nm
- 2020, ~256 cores, 6nm
- 2022, ~512 cores, 4nm
- 2024, ~1024 cores, 3nm
- 2026, ~2048 cores, 2nm
- *scale discontinuity?*
- 2028, ~4096 cores
- 2030, ~8192 cores
- 2032, ~16384 cores

Summary

- Single core performance hit a plateau in the mid 2000s
- To address that issue constructors started to pack more cores on a single chip
- Next: **how to efficiently exploit the resulting parallelism**?